

Ground Bounce Demonstration Board

Introduction:

The 3"x3" experiment board attempts to demonstrate *ground bounce* and V_{CC} *bounce*, the effects of capacitor discharge through the totem-pole outputs of a logic gate.

Background:

Ground bounce is a troublesome and important concept to consider since it may hinder the correct operation of a logic circuit by violating voltage margins. This effect is caused by the inductance of the lead that connects the *board ground* and *chip ground*. Figure 1 shows the elements involved. Ground bounce occurs on the transition from logic 1 to logic 0 and vice versa, i.e. when the capacitor is charged and discharged.

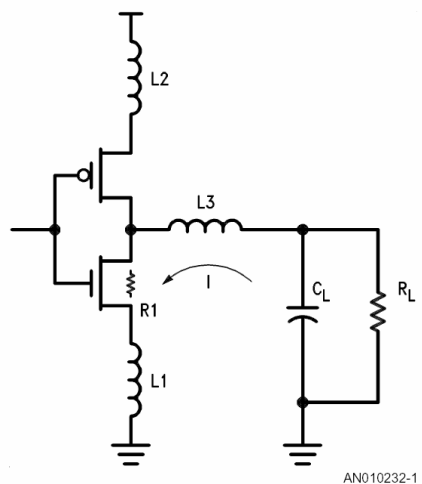


Figure 1. Current I caused by the discharge of C_L induces voltage on L_1 creating a difference between board and chip ground [1].

Without getting into much detail, the magnitude of ground bounce depends on the rate of change of the voltage and rate of change of current as follows:

$$I = -C_L \cdot (dV/dt) \text{ and } V_{GB} = L_1 \cdot (dI/dt) \quad [1]$$

The current is accumulated linearly with the number of simultaneously switching outputs (same transition).

The effects of ground bounce are also observed in chip V_{CC} , however, due to higher noise margins at the top rail, the effects of V_{CC} bounce are less dire on the logic [1].

Please refer to [1] for an excellent discussion on ground/ V_{CC} bounce, causes and solutions.

Experiment:

The intent of the experiment is to observe GB and how different connections to ground and power planes affect the observations. The active part needed to charge and discharge a load capacitor and to be considerably fast in order to maximize dV/dt . In addition, the part should have as much outputs as possible to maximize the current flowing through the ground pin. The 9bit transparent latch, 74F843 [2], was chosen for the task. The part's 24 pin package enabled connecting the clock to the $nCLEAR$ and $LATCH ENABLE$ pins and the inputs to V_{CC} to achieve the appropriate transitions. Measured **rise time of $\sim 7ns$** .

In order to observe GB and V_{CC} bounce two outputs are used to look into chip ground and chip V_{CC} using a 21:1 probe. The rest of the seven outputs are connected to capacitive loads of 100pF. This capacitance was chosen to dramatize the GB effect (more current) and is beyond the recommended load on the part. The attached schematics show all connections. The loads could be disconnected in order to view the effects of adding loads on GB.

The design enables four different connections to the power planes:

1. **Via (GND) or direct (V_{CC})**
2. **50mil trace**
3. **8mil trace**
4. **Wire wrap (w/w)**

Remember that all of the above is connected through a header jumper yielding more imperfections to the connection. The expectation is that the observed GB will increase going down the above list.

Results:

Ground bounce was observed in all cases. V_{CC} bounce was not observed because the chip V_{CC} is shorted to ground on reset ($nCLEAR$) and therefore does not stay at V_{CC} throughout all transitions. I focused on GB and fixed V_{CC} connection directly to plane.

A frequency of 10kHz was chosen to allow the capacitors to fully charge.

For each connection to ground from the above list I started with one load and ended with 7 capacitive loads. With each additional load capacitor the GB increased by approximately 0.2V. Since the measurements were taken with a 21:1 probe the figures below reflect a multiplication of the scope's measurements. The following are figures of logic 1 to logic 0 transitions (approximate):

GND Connection	GB min (1) load, V	GB max (7) load, V
Via	0.6	1.8
50mil	0.8	2.2
8mil	0.8	2.2
w/w	0.8	2.3

The magnitude relations adhere to the expectations; however, the actual numbers are quite a bit more than I expected. Also surprising is the non-existent differences in GB between the w/w thin and thick connection to ground; they seem to be identically bad.

The excerpt below from the 74F843 data sheet shows the allowed (noise) margins, V_{IH} (min 2V) and V_{IL} (max 0.8V) which are typical TTL. It is evident that the observed GB would render the proper logic operation of this family as it would switch beyond V_{IH} .

DC Electrical Characteristics							
Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage			-1.2	V	Min	$I_{IN} = -18$ mA
V_{OH}	Output HIGH Voltage	10% V_{CC}	2.5		V	Min	$I_{OH} = -1$ mA
		10% V_{CC}	2.4				$I_{OH} = -3$ mA
		5% V_{CC}	2.7				$I_{OH} = -1$ mA
		5% V_{CC}	2.7				$I_{OH} = -3$ mA
V_{OL}	Output LOW Voltage			0.5	V	Min	$I_{OL} = 24$ mA

Figure 2. Noise margins in 74F843 [2].

The GB waveforms are peak and the ring until they level to approximately midway voltage, then decay slowly back to ground. I could not find a reference to this in the literature and it might be some parasitic effect in my setup, but since the spike is so short, it might be that only the midway level is noticed, minimizing the GB's harm. Different setups yield different decay patterns; however, the general form is the same.

Observation: As stated, V_{CC} was not observable; however, when connecting V_{CC} through wire wrap, as opposed to a direct connection to the plane, the ground bounce magnitude shifts upwards by $0.2V - 0.4V$.

Conclusion:

Direct connection to a ground/ V_{CC} plane is best to avoid logic failures due to GB. One should also calculate the GB due to trace inductance and voltage swing if no direct connection is available. It should also be realized that the more *simultaneously switching outputs* (SSO), GB gets worse; if a design does not have many SSO's GB might not be a grave danger.

This was a highly educational process with great value. I believe every engineer should have this hands-on experience before being unleashed to industry. For myself, I came with previous knowledge that helped me quite a bit. For others, judging from their questions, I think more guidance was needed with regards to the finer details. A simple list of do's and don'ts would suffice to make process smoother (example item: "*don't use the auto-router?*"). It is a fine line between giving too much guidance and too little. Too much spoils the fun and makes it too easy and too little people complain that it is too hard.

Thanks.

Design and Layout Issues:

- The drill of 125mils does not fit the standard standoffs and I needed to drill larger holes.
- I neglected to account for the space the standoffs would take and had to scrape out a plane corner and maneuver around one of them which had a pin very close to it.
- All through hole connections in the board were erroneously connected to the ground plane. This is due to the shifting of the Gerber files on the larger board sent to the board house.
- The ground plane covered only half of the bottom layer. I can not recall why I did that, but in retrospect, I would have covered the whole bottom layer with copper.
- There was no chip or plane bypassing (*sigb*). I added a 47uF tantalum capacitor between power and ground inputs which took all ringing away (really nice). In addition, I bypassed the 74F843 with a ceramic 0.1uF capacitor which did not show dramatic improvement.

References:

- [1] <http://www.fairchildsemi.com/an/AN/AN-640.pdf>
- [2] <http://www.fairchildsemi.com/ds/74/74F843.pdf>